REMARKS

Reconsideration of the application, as amended, is respectfully requested.

I. STATUS OF THE CLAIMS

Claims 1-33 are currently pending.

II. OBJECTION TO THE SPECIFICATION

The disclosure has been objected to on the grounds that throughout the present specification, the bit line and the parts related to the bit line are followed by part numbers (600, 610, 650 and 660) not noted in the figures being discussed.

In response, the above objected to portions of the specification have been amended herewith such that the appropriate figures which depict parts 600, 610, 650 and 660 are now also referred to in these portions of the specification.

No new matter has been added by virtue of this amendment. It is believed that in view of the above action taken, the above objection has been obviated. Therefore, withdrawal of the above rejection is requested.

III. 35 U.S.C. 112, SECOND PARAGRAPH REJECTIONS

Claims 1-3, 13-14, 21, 23 and 28-29 have been rejected under 35 U.S.C. 112, second paragraph on the grounds that the expression " in a direction of" recited in these claims renders these claims indefinite.

In response, Applicants note that, for example, **Figs. 2A-10C of the present application**, illustrate an exemplary embodiment of the present invention which depicts directions in which each element recited in claims 1-3, 13-14, 21, 23 and 28-29 may be formed. Moreover, for example, **pages 10-18 of the present specification**, while describing an exemplary embodiment

of the present invention also discusses directions in which each element recited in claim 1-3, 13-14, 21, 23 and 28-29 may be formed. Thus, one skilled in the art based upon the above figures, the present specification as a whole and their knowledge of the semiconductor manufacturing art would clearly understand the scope of the expression "in a direction of" as recited in claims 1-3, 13-14, 21, 23 and 28-29.

Withdrawal of the above rejection to claims 1-3, 13-14, 21, 23 and 28-29 is therefore requested.

III. 35 U.S.C. 102(e) REJECTIONS

(i) Claims 1-4, 6-12, 15-18, 21-27, 30 and 31 have been rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,403,413 to Hayano et al. ("the Hayano patent").

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. **(See MPEP 2133, Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).**

Hayano at the very least fails to teach or suggest all of the features recited in claims 1 and 21.

In particular, Hayano at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes selectively etching a third insulating layer (claim 1) or insulating layer (claim 21) to form a band-type opening, wherein the band-type opening crosses the bit lines and exposes the first contact pads as recited in claims 1 and 21. Additionally, Hayano also at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes patterning the conductive layer to form individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer (claim 1) or insulating layer (claim 21) in a direction of the

bit line and a body that is electrically connected to a first contact pad, as recited in claims 1 and 21.

It appears that in the instant Office Action, the contact holes 17 described in Hayano are being equated to the band-type openings recited in claims 1 and 21. **(See page 4, lines 11-13 of the instant Office Action).** However, it is respectfully asserted that these contact holes 17 formed in Hayano are clearly not band-type openings as recited in claims 1 and 21. **(See, for example, band-type openings 531 of an exemplary embodiment of the present invention illustrated in Figs. 7B, 8B, 9B, 10B and 10C of the present specification).** Moreover, the contact holes 17 in Hayano are not formed to cross bit lines as recited in claims 1 and 21. Rather, in Hayano, these contact holes 17 are formed to penetrate layers 15, 16 and 12 but clearly do not cross the data lines DL as required by claims 1 and 21(**See Figs. 25-28, Figs, 36-37, and Col.15-Col. 16, lines 1-7 of Hayano).** Thus, Hayano at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes selectively etching a third insulating layer (claim 1) or insulating layer (claim 21) to form a band-type opening, wherein the band-type opening crosses the bit lines and exposes the first contact pads as recited in claims 1 and 21.

Furthermore, it also appears that in the instant Office Action, the plugs 19 described in Hayano are being equated to the contact bodies which each include an extension recited in claims 1 and 21. **(See pages 4-5 of the instant Office Action).** However, it is respectfully asserted that these plugs 19 formed in Hayano are clearly not contact bodies which each include an extension as recited in claims 1 and 21. **(See, for example, contact bodies 810 of an exemplary embodiment of the present invention illustrated in Figs. 9B, 10B and 10C of the present specification).** Rather, the plugs 19 in Hayano are formed without including any extensions **(See Figs. 36-37 of Hayano).** Therefore, Hayano also at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes patterning the conductive layer to form individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer (claim 1) or insulating layer (claim 21) in a direction of the bit line and a body that is electrically connected to a first contact pad, as recited in claims 1 and 21.

Accordingly, Hayano fails to teach or suggest all of the method steps recited in claims 1 and 21 and thus fails to anticipate these claims as well. Therefore, withdrawal of the above rejections to claims 1 and 21 is respectfully requested.

As claims 6-12 and15-18 depend from and incorporate all of the limitations of claim 1 and claims 22-27, 30 and 31 depend from and incorporate all of the limitations of claim 21, withdrawal of the rejection to these dependent claims is likewise requested.

III. 35 U.S.C. 103(a) REJECTIONS

(i) Claims 5, 13, 14, 28 and 29 have been rejected under 35 U.S.C. 103(a) as being obvious over Hayano (as discussed above) in view of U.S. Patent Application Publication No. 2001/0045589 to Takeda et al.

To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. **(See MPEP 2143.03; In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)).**

As noted above, Hayano at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes selectively etching a third insulating layer (claim 1) or insulating layer (claim 21) to form a band-type opening, wherein the band-type opening crosses the bit lines and exposes the first contact pads as recited in claims 1 and 21. Additionally, as noted above, Hayano also at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes patterning the conductive layer to form individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer (claim 1) or insulating layer (claim 21) in a direction of the bit line and a body that is electrically connected to a first contact pad, as recited in claims 1 and 21. As claims 5, 13 and 14 depends from and incorporates all of the limitations of claim 1 and claims 28 and 29 depend from and incorporate all of the limitations of claim 21, Hayano also fails to teach or suggest all of the features recited in these dependent claims as well.

Furthermore, it is submitted that the Examiner has failed to meet his initial burden of establishing a prima facie case of obviousness. In addition, the combination of Hayano and Takeda fails to teach or suggest all of the features recited in claims 5, 13, 14, 28 and 29.

(a) Failure to Meet Initial Burden of Establishing Prima Facie Case of Obviousness

As is well known under U.S. Patent Law, the Examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. **(See MPEP 2142).** In particular, the instant Office Action is completely silent regarding what the actual teachings of the Takeda reference are and/or where to find these teachings within the Takeda reference. **(See pages 9-11 of the instant Office Action).** In other words, the Takeda reference has simply been cited in combination with the Hayano reference without an explanation of what Takeda actually teaches and where to find these teachings within the reference.

(b) Failure to Teach or Suggest all of the Features of Claims 5, 13, 14, 28 and 29

Nevertheless, Takeda as with Hayano fails to teach or suggest methods for manufacturing semiconductors which includes the forming of band-type opening crossing the bit lines and/or forming individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer (claim 1) or insulating layer (claim 21) as recited in claims 5, 13, 14, 28 and 29. Therefore, even if Takeda were combined with Hayano, this combination would still fail to teach or suggest all of the limitations recited in claim 23.

Therefore, withdrawal of the above rejection to claims 5, 13, 14, 28 and 29 is respectfully requested.

(ii) Claims 19, 20, 32 and 33 have been rejected under 35 U.S.C. 103(a) as being obvious over Hayano (as discussed above) in view of U.S. Patent Application Publication No. 2001/0041406 to Goebel et al. ("the Goebel publication").

As noted above, Hayano at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes selectively etching a third insulating

layer (claim 1) or insulating layer (claim 21) to form a band-type opening, wherein the band-type opening crosses the bit lines and exposes the first contact pads as recited in claims 1 and 21. Additionally, as noted above, Hayano also at the very least fails to teach or suggest a method for manufacturing a semiconductor device, which includes patterning the conductive layer to form individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer (claim 1) or insulating layer (claim 21) in a direction of the bit line and a body that is electrically connected to a first contact pad, as recited in claims 1 and 21. As claims 19 and 20 depends from and incorporates all of the limitations of claim 1 and claims 32 and 33 depend from and incorporate all of the limitations of claim 21, Hayano also fails to teach or suggest all of the features recited in these dependent claims as well.

Moreover, even if the alleged teachings of Goebel with regard to methods for molding electrodes were combined with Hayano in the manner proposed in the instant Office, this combination would still fail to teach or suggest all of the limitations recited in claim 19, 20, 32 and 33. In particular, the above combination of Goebel with Hayano at the very least fails to teach or suggest a methods for manufacturing semiconductors which includes the forming of band-type opening crossing the bit lines and/or forming individual storage electrode contact bodies, wherein each of the contact bodies includes an extension that is extended on the third insulating layer (claim 1) or insulating layer (claim 21) as recited in claims, as recited in claims 19, 20, 32 and 33.

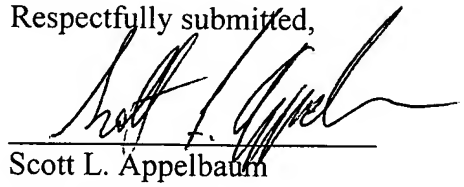
Therefore, withdrawal of the above rejection to claims 19, 20, 32 and 33 is respectfully requested.

IV. CONCLUSION:

For the foregoing reasons, the present application, including claims 1-33, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully

requested. The Examiner is invited to contact the undersigned if he has any questions or comments in this matter.

Respectfully submitted,



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